

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Fitzgerald, et al.

GROUP: 2823

SERIAL NO: 10/603,850

EXAMINER: Belur V. Keshava

FILED: 06/25/2003

Date of mailing
of Notice ofFOR: COPLANAR INTEGRATION OF
LATTICE-MISMATCHED SEMICONDUCTOR
WITH SILICON VIA WAFER BONDING VIRTUAL
SUBSTRATES

Allowance: 3/28/2005

Mail Stop Issue Fee
Assistant Commissioner of Patents
P.O. Box 1450, Alexandria, VA 22313-1450

Attn: Official Draftsman

TRANSMITTAL OF FORMAL DRAWINGS

Applicant submits herewith new drawing(s) for this application. Attached please find twelve (12) sheets of formal drawings for this application.

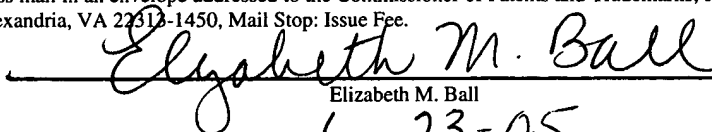
The three month period of response set in the Notice of Allowability (PTOL 37) expires on June 28, 2005 and this submission is on or before this expiry date.

Respectfully submitted,



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I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the Commissioner of Patents and Trademarks, P.O. Box 1450, Alexandria, VA 22313-1450, Mail Stop: Issue Fee.



Elizabeth M. Ball

Date: 6-23-05